REMARKS

This is intended as a full and complete response to the Final Office Action dated October 3, 2006, having a shortened statutory period for response set to expire on January 3, 2007. Please reconsider the claims pending in the application for at least the reasons discussed below.

Claims 1, 3-12, 14-19, and 21-26 remain pending in the application and are shown above. Claims 1, 3-12, 14-19, and 21-26 are rejected. Reconsideration of the rejected claims is requested for the reasons presented below.

Applicants propose amending claims 1, 12, and 19 to more clearly illustrate the claimed subject matter. Applicants submit that the changes proposed herein do not introduce new matter. Applicants respectfully request entry of the proposed amendments.

Claims 1, 3-12, and 14-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yang, et al.* (U.S. Patent No. 6,734,559) in view of *Gates, et al.* (U.S. Patent No. 6,203,613). The Examiner states that *Yang, et al.* teaches a method comprising depositing a barrier layer in a feature in a dielectric layer of a substrate, filling the feature with a metal-containing layer, planarizing the substrate, and depositing a refractory metal nitride cap layer on the substrate. The Examiner acknowledges that *Yang, et al.* does not disclose depositing the cap layer by a cyclical deposition process comprising alternately pulsing a metal-containing compound and a nitrogen-containing compound to deposit the refractory metal nitride cap layer and notes that *Gates, et al.* teaches the deposition of a metal nitride layer by atomic layer deposition. The Examiner asserts that it would have been obvious to deposit *Yang, et al.'s* refractory metal nitride cap layer by atomic layer deposition according to the teachings of *Gates, et al.* Applicants respectfully traverse the rejection.

As amended, claim 1 recites a method that comprises planarizing a substrate to create a planar surface comprising a surface of a dielectric layer and a surface of a metal-containing layer and depositing a refractory metal nitride cap layer on the planar surface of the substrate. *Yang, et al.* describes planarizing a channel 201 and then etching the surface of the channel back such that the channel and dielectric layer 226

are not co-planar when the barrier 206 is deposited on the channel and dielectric layer (column 4, lines 25-37, Figures 3 and 4). Applicants respectfully submit that *Yang, et al.*, individually or in combination with *Gates, et al.*, does not teach or suggest planarizing a substrate to create a planar surface comprising a surface of a dielectric layer and a surface of a metal-containing layer and depositing a refractory metal nitride cap layer on the planar surface.

Thus, *Yang, et al.* in view of *Gates, et al.* does not teach, show, or suggest a method for forming a cap layer, comprising depositing a barrier layer in a feature in a dielectric layer of a substrate, filling the feature with a metal-containing layer, planarizing the substrate to create a planar surface comprising a surface of the dielectric layer and a surface of the metal-containing layer, and depositing a refractory metal nitride cap layer on the planar surface of the substrate by a cyclical deposition process comprising alternately pulsing a metal-containing compound and a nitrogen-containing compound to deposit the refractory metal nitride cap layer, as recited in amended claim 1. Applicants respectfully request withdrawal of the rejection of claim 1 and of claims 3-11, which depend thereon.

Regarding claim 12, Applicants note that amended claim 12 also recites a method comprising planarizing a substrate to create a planar surface comprising a surface of a dielectric layer and a surface of a metal-containing layer and depositing a refractory metal nitride (*i.e.*, tantalum nitride) cap layer on the planar surface of the substrate. Thus, for the reasons discussed above with respect to claim 1, Applicants respectfully submit that *Yang, et al.* in view of *Gates, et al.* does not teach or suggest all of the elements of amended claim 12. Applicants respectfully request withdrawal of the rejection of claim 12 and of claims 14-18, which depend thereon.

Claims 19 and 20-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yang, et al.* in view of *Gates, et al.* as applied to claims 1, 3-11, and 13-18 above, and further in view of *Naik, et al.* (U.S. Patent No. 6,204,168). The Examiner states that *Yang, et al.* in view of *Gates, et al.* teaches a method of forming a dual damascene structure comprising depositing a first dielectric film on a substrate, depositing an etch stop on the first dielectric film, depositing a second dielectric film on the etch stop and the exposed first dielectric film, etching the second dielectric film to

define a horizontal interconnect and a vertical interconnect, depositing a barrier layer on the substrate, depositing a metal-containing layer on the substrate to fill the vertical interconnect and the horizontal interconnect, planarizing the metal-containing layer and the second dielectric film, depositing a refractory metal nitride cap layer on the planarized metal-containing layer and the planarized second dielectric film by a cyclical deposition process, and depositing an etch stop layer on the refractory metal nitride cap layer. The Examiner acknowledges that *Yang, et al.* in view of *Gates, et al.* does not state the method in which the dual damascene trenches are formed. The Examiner notes that *Naik, et al.* teaches a dual damascene method (Figure 1) and asserts that it would have been obvious to combine the teachings of *Yang, et al.* in view of *Gates, et al.* and *Naik, et al.* to enable the method of dual damascene opening formation to be performed according to the teachings of *Naik, et al.* Applicants respectfully traverse the rejection.

Applicants propose amending claim 19 to clarify that "depositing a metal-containing layer on the substrate to fill the vertical interconnect and the horizontal interconnect" refers to depositing a metal-containing layer that fills both a vertical interconnect and a horizontal interconnect. Applicants submit that the proposed amendment to claim 19 does not raise new issues, as claim 19 already recites a method of forming a dual damascene structure, which inherently includes depositing a metal-containing layer that fills both a vertical interconnect and a horizontal interconnect.

Applicants agree that Figure 1 of *Naik, et al.* shows a dual damascene process. However, Applicants respectfully submit that *Yang, et al.* in view of *Gates, et al.* and *Naik, et al.* does not teach, suggest, or provide a reasonable expectation of success for using *Naik, et al.'s* dual damascene process to form the structure of *Yang, et al.* In *Yang, et al.'s* structure, metal layers 210 and 201 are separated from each other by barrier layer 221 and seed layer 222 (Figure 3). Thus, Applicants submit that there is no reasonable expectation of success for using *Naik, et al.'s* dual damascene process in which a metal layer simultaneously fills both a vertical interconnect and a horizontal interconnect (column 7, lines 4-14 of *Naik, et al.*) to form the structure of *Yang, et al.*, as the interconnects of *Yang, et al.* are separated by a barrier layer and a seed layer.

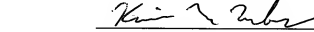
Therefore, *Yang, et al.* in view of *Gates, et al.* and *Naik, et al.* does not teach, show, or suggest a method of forming a dual damascene structure, comprising depositing a first dielectric film on a substrate, depositing an etch stop on the first dielectric film, pattern etching the etch stop to define a vertical interconnect opening and expose the first dielectric film, depositing a second dielectric film on the etch stop and the exposed first dielectric film, pattern etching the second dielectric film to define a horizontal interconnect and continuing to etch the exposed first dielectric film to define the vertical interconnect, depositing a barrier layer on the substrate, depositing a metal-containing layer on the substrate to fill both the vertical interconnect and the horizontal interconnect, planarizing the metal-containing layer and the second dielectric film, depositing a refractory metal nitride cap layer on the planarized metal-containing layer and the planarized second dielectric film by a cyclical deposition process comprising alternately pulsing a metal-containing compound and a nitrogen-containing compound to deposit the refractory metal nitride cap layer, and depositing an etch stop layer on the refractory metal nitride cap layer, as recited in amended claim 19. Applicants respectfully request withdrawal of the rejection of claim 19 and of claims 20-26, which depend thereon.

In conclusion, the references cited by the Examiner, alone or in combination, do not teach, show, or suggest the invention as claimed.

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the Final Office Action. Therefore, Applicants believe that a detailed discussion of the secondary references is not necessary for a full and complete response to this Final Office Action.

Having addressed all issues set out in the Final Office Action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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